In the Claims

CLAIMS

Claims 1-68 (cancelled).

69 (Currently amended): A CMOS, comprising:

a dielectric layer over a substrate;

a PMOS gate and an NMOS gate over the dielectric layer;

a first metal-containing material within the PMOS gate and over the dielectric layer, the first metal-containing material having a thickness of greater than 20Å;

a second metal-containing material within the NMOS gate and over the dielectric layer, the second metal-containing material having a thickness of less than or equal to about 20Å;

a first layer ~~of~~ comprising n-type doped silicon within the PMOS gate and over the first metal-containing material; and

a second layer ~~of~~ comprising n-type doped silicon within the NMOS gate and over the second metal-containing material.

70 (original): The CMOS of claim 69 wherein the dielectric layer comprises one or more of tantalum, hafnium and aluminum.

71 (original): The CMOS of claim 69 wherein the dielectric layer comprises aluminum oxide.

72 (original): The CMOS of claim 71 wherein the first and second metal-containing materials are physically against the aluminum oxide.

73 (original): The CMOS of claim 69 wherein the first and second metal-containing materials have the same composition as one another.

74 (original): The CMOS of claim 73 wherein the first and second metal-containing materials predominately comprise one or more of titanium nitride, tantalum nitride, tungsten nitride and hafnium nitride.

75 (original): The CMOS of claim 73 wherein the first and second metal-containing materials predominately comprise one or more of titanium silicide, tantalum silicide, tungsten silicide and hafnium silicide.

76 (original): The CMOS of claim 69 wherein the thickness of the second metal-containing material is less than or equal to about 15Å.

77 (original): The CMOS of claim 69 wherein the thickness of the second metal-containing material is less than or equal to about 10Å.

78 (original): The CMOS of claim 69 wherein the thickness of the first metal-containing material is greater than or equal to about 100Å.

79 (original): The CMOS of claim 69 wherein the thickness of the first metal-containing material is greater than or equal to about 150Å.

80 (original): The CMOS of claim 69 wherein the thickness of the first metal-containing material is greater than or equal to about 150Å, and wherein the thickness of the second metal-containing material is less than or equal to about 15Å.

81 (Currently amended): An electronic system comprising:

a processor; and

a memory device electrically coupled with the processor; and

wherein at least one of memory device and processor includes a CMOS comprising:

a dielectric layer over a substrate;

a PMOS gate and an NMOS gate over the dielectric layer;

a first metal-containing material within the PMOS gate and over the dielectric layer, the first metal-containing material having a thickness of greater than 20Å;

a second metal-containing material within the NMOS gate and over the dielectric layer, the second metal-containing material having a thickness of less than or equal to about 20Å;

a first layer ~~of~~ comprising n-type doped silicon within the PMOS gate and over the first metal-containing material; and

a second layer ~~of~~ comprising n-type doped silicon within the NMOS gate and over the second metal-containing material.

Claims 82-94 (cancelled).

95 (New): The CMOS of claim 69 wherein the first metal-containing material comprises a first composition, and wherein the second metal-containing material comprises a second composition different from the first composition.

96 (New): The electronic system of claim 81 wherein the first metal-containing material comprises a first composition, and wherein the second metal-containing material comprises a second composition different from the first composition.